DC OFFSET AND 1/f NOISE COMPENSATION OF A DIRECT CONVERSION RECEIVER

BACKGROUND OF THE INVENTION

Field of the Invention: This invention relates to a radio receiver, in particular to a direct conversion receiver with zero intermediate frequency.

Brief Description of Related Art: In recent years, the direct conversion radio receiver has gained a great deal of interest. In such a receiver, the incoming signal is mixed with a local oscillator of the same frequency, and the beat frequency intermediate frequency (IF) signal has zero frequency (i.e. a DC signal). There is no image to reject and there is no need for a front-end image reject filter. Nor is there any need for an external filter such as a surface acoustic wave (SAW) filter for the IF signal.

However, there are several drawbacks to direct conversion. Among these problems is sensitivity to DC offsets (both internal as well as externally induced) and 1/f noise: With zero IF, the DC offsets and 1/f noise represent error components within the same band as the desired signal.

Many attempts have been made to overcome these problems. [1, 2]. Most of these solutions use some negative feedback schemes, which are complicated, sensitive to instability, and may not solve both the DC offset and 1/f problem together.

SUMMARY OF THE INVENTION

An object of the present invention is to compensate for the DC offset problem in a direct conversion receiver. Another object is to minimize the 1/f noise in a direct conversion receiver. Still another object of the present invention is to overcome the DC offset problem and the 1/f problem simultaneously.

These objects are achieved by means of double sampling. During the first sampling period, the DC offset and 1/f noise signal are sampled as a compensation signal without any RF signal input and stored in a capacitor. During the second sampling period, the RF signal is applied and the stored DC offset and 1/f noise signal is connected in opposite phase in series with the RF signal, thus canceling the stored DC offset and the 1/f noise.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows the basic block diagram of the present invention using double sampling technique for DC offset and 1/f noise compensation in direct conversion receiver..

Fig. 2 shows the basic circuit for implementing the doubling sampling compensation of DC offset and 1/f noise.

Fig.3a shows a calibration signal applied after the low noise amplifier; Fig.3b shows a calibration signal applied after the mixers; and Fig.3(c) shows a calibration signal applied after the low-pass filter.

Fig. 4 shows the application of double sampling compensation to multiple number of stages of the zero intermediate frequency (IF) amplifier.

DETAILED DESCRIPTION OF THE INVENTION

Fig.1 shows the basic block diagram of the present invention as applied to a direct conversion receiver. Normally the receiver operates the single-pole, double-throw (SPDT) switches S1, S2, S3 in position "b". The incoming signal Vin is amplified by a low-noise amplifier LNA. The amplifier signal from the LNA is mixed with a local oscillator (LO) with the same frequency as the incoming signal Vin. The local oscillator generates an in-phase component I and a quadrature component Q. The I component and the Q component beat with the amplified incoming signal from the LNA in the mixers MXI and MXQ respectively to produce two zero frequency (i.e. DC) IF signals. The signal from MXI is filtered by a low-pass filter LPI, and the signal from MXQ is filtered by low-pass filter LPQ to eliminate any double frequency image signals. The filtered signals LPI and LPQ are then amplified by amplifiers VGAI and VGAQ respectively before demodulation. Since VGAI and VGAQ are DC amplifiers, the DC offset voltage and 1/f noise pose serious problems.

Such DC offset voltage and 1/f noise are compensated by double-sampling in Fig.1. The amplifiers are first calibrated during phase "a" with the SPDT switches S1, S2 and S3 switched to position "a". During phase "a", the DC offset voltage and the 1/f noise required for compensation is measured and stored in the compensation blocks, "Offset compensation". During phase "b" with the switches S1, S2 and S3 in position "b", the stored DC offset voltage and the 1/f noise during phase "a" are applied in opposite direction to compensate for the DC offset voltage and 1/f noise voltage when the switches are in position "b".

Fig.2 shows the basic compensation circuit for storing the compensation voltages. A double-sampled signal V2 is applied to the input of this compensation circuit. V2 contains a calibration signal which is applied during the calibration phase corresponding to position "a" of all the SPDT switches S4, S5 and S6 and a signal-flow phase corresponding to position "b" of all the switches. The amplifier A1 corresponds to either VGAI or VGAQ in Fig.1 and is an operational amplifier. The inverting input terminal is short-circuited to the output through a SPDT S6 in position "a" during the calibration phase , and is connected through capacitor C1, which is grounded through S4.

Meanwhile, V2 is applied to the non-inverting terminal of the operational amplifier through a low-pass filter LP2 and switch S5. In this connection, any DC offset voltage and 1/f noise signal in V2 appears at the non-inverting terminal of A1, which, in turn, appears at the inverting terminal due to virtual ground. Thus the capacitor C1 is charged up to the DC offset voltage plus the 1/f noise voltage. During the signal phase of V2 corresponding position "b" of all the switches, the signal in V2 is applied through C1 to the inverting terminal of A1, which now operates normally. Since the stored DC offset voltage plus the 1/f noise voltage stored in C1 opposes the DC offset voltage in V2, the DC offset voltage and 1/f noise voltage are canceled, and not amplified by A1.

The compensation circuit can be applied at any point before the zero IF amplifiers. Fig. 1 shows the application of the compensation circuit at node N before the LNA amplifier. The compensation circuit can also be applied to node D after the LNA amplifier as shown in Fig. 3(a), after the mixers MXI, MXQ at nodes E, F as shown in Fig.3(b), or after the low-pass filters LPI, LPQ at nodes G,H as shown in Fig.3(c).

Fig.1 is shown for a single stage of the IF amplifier VGAI and VGAQ. If the IF amplifier has more than one stage, the compensation can be applied to the last stage or individually to every stage. For application to more than one stage individually such as VGA1, VGA2 using SPDT switches such as S21, S22, etc., the compensation circuit Fig.3(c) can be repeated as shown in Fig.4.

The calibration signal can be of DC or an RF signal to simulate a regular situation, or any other AC signal. When a DC calibration signal is used, the low pass filter LP shown in Fig.1 need not be used.

The use double sampling may incur charge injection and parasitic capacitance problems. Such problems have been known and solved by those skilled in the art, and not elaborated.

While the preferred embodiments of the invention have been described, it will be obvious to those skilled in the art that various modifications may be made to the invention without departing from the spirit of the present invention. Such modifications are all within the scope of the present invention.